National Semiconductor

May 2005

LM2425
220V Monolithic Triple Channel 10 MHz CRT DTV Driver

General Description

The LM2425 is a triple channel high voltage CRT driver circuit designed for use in DTV applications. The IC contains three high input impedance, wide band amplifiers which directly drive the RGB cathodes of a CRT. Each channel has its gain internally set to –53 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation.

The IC is packaged in an industry standard 11-lead TO-220 molded plastic power package designed specifically to meet high voltage spacing requirements. See Thermal Considerations section.

Features

- 10 MHz bandwidth at $130V_{PP}$ output swing
- Up to $170V_{PP}$ output swing with AC coupling to cathodes
- 0V to 5V input voltage range
- Stable with 0 pF–20 pF capacitive loads and inductive peaking networks
- Convenient TO-220 staggered thin lead package style

Applications

- AC or DC coupled DTV applications.

Connection Diagram

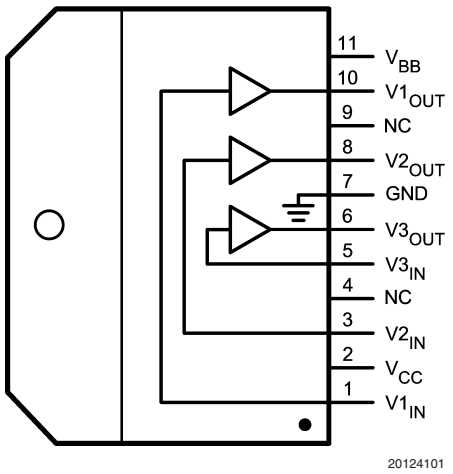

FIGURE 1. Top View
Order Number LM2425TE
See NS Package Number TE11B NOPB
Available only with lead free plating

Schematic Diagram

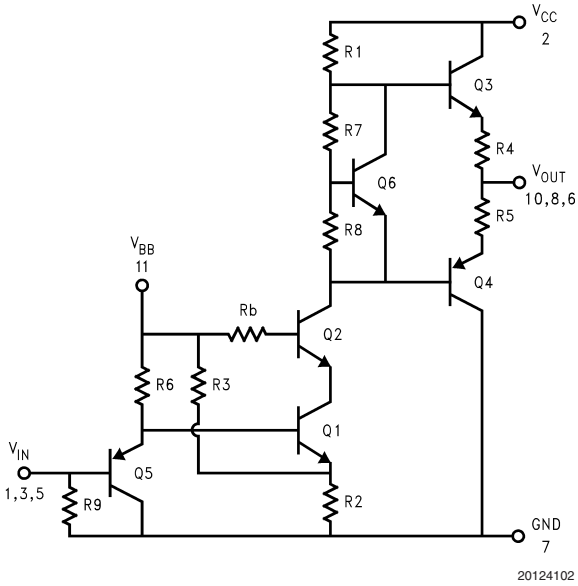

FIGURE 2. Simplified Schematic Diagram (One Channel)

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Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	+250V
Bias Voltage (V_{BB})	+16V
Input Voltage (V_{IN})	−0.5V to V_{BB} +0.5V
Storage Temperature Range (T_{STG})	−65˚C to +150˚C
Lead Temperature	
(Soldering, <10 sec.)	300˚C
ESD Tolerance,	
Human Body Model	2 kV
Machine Model	200V
Junction Temperature	150˚C
θ_{JC} (typ)	2.75˚C/W

Operating Ratings (Note 2)

V_{CC}	+100V to +230V
V_{BB}	+7V to +13V
V_{IN}	+0V to +5V
V_{OUT}	+40V to +215V
Case Temperature	110˚C

Do not operate the part without a heat sink.

Electrical Characteristics

(See *Figure 2* for Test Circuit) Unless otherwise noted: V_{CC} = +220V, V_{BB} = +12V, C_L = 10 pF, T_C = 50˚C. DC Tests: V_{IN} = +2.70V_{DC}. AC Tests: Output = 130V_{PP} (60V − 190V) at 1 MHz.

Symbol	Parameter	Conditions	LM2425			Units
			Min	Typ	Max	
I_{CC}	Supply Current	No Input Signal, No Video Input, No Output Load	10	17	25	mA
I_{BB}	Bias Current		5	13	18	mA
$V_{OUT, 1}$	DC Output Voltage	No AC Input Signal, V_{IN} = 2.70V_{DC}	121	127	133	V_{DC}
$V_{OUT, 2}$	DC Output Voltage	No AC Input Signal, V_{IN} = 1.20V_{DC}	199	205	211	V_{DC}
A_V	DC Voltage Gain	No AC Input Signal	−50	−53	−56	V/V
ΔA_V	Gain Matching	(Note 4), No AC Input Signal		1.0		dB
LE	Linearity Error	(Notes 4, 5), No AC Input Signal		8		%
t_r	Rise Time, 60V to 190V	(Note 6), 10% to 90%		33		ns
+OS	Overshoot			8		%
t_f	Fall Time, 60V to 190V	(Note 6), 90% to 10%		38		ns
−OS	Overshoot	(Note 6)		4		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

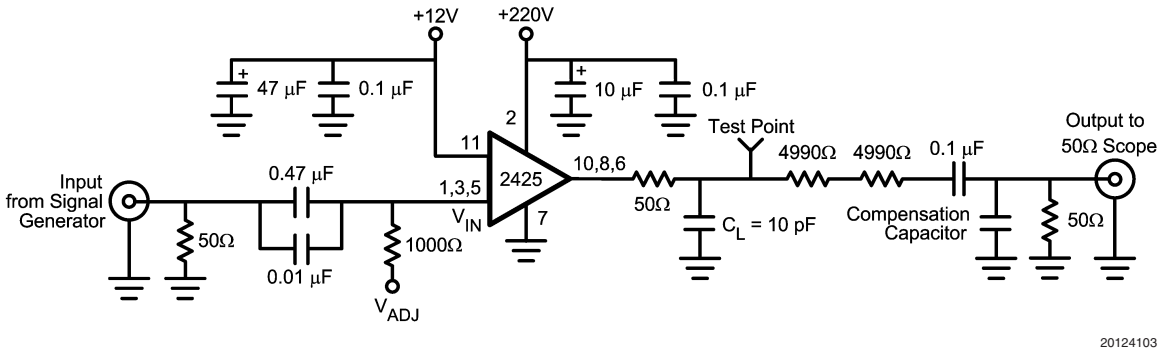
Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Calculated value from Voltage Gain test on each channel.

Note 5: Linearity Error is the variation in DC gain from V_{IN} = 1.10V to V_{IN} = 4.30V.

Note 6: Input from signal generator: t_r, t_f < 1 ns.

AC Test Circuit



Note: 10 pF load includes parasitic capacitance.

FIGURE 3. Test Circuit (One Channel)

Figure 3 shows a typical test circuit for evaluation of the LM2425. This circuit is designed to allow testing of the LM2425 in a 50Ω environment without the use of an expensive FET probe. The two 4990Ω resistors form a 400:1 divider with the 50Ω resistor and the oscilloscope. A test point is included for easy use of an oscilloscope probe. The compensation capacitor is used to compensate the network to achieve a flat frequency response.

Typical Performance Characteristics

(V_{CC} = +220V_{DC}, V_{BB} = +12V_{DC}, C_L = 10 pF, V_{OUT} = 130V_{PP} (60V – 190V), T_C = 50˚C, Test Circuit — *Figure 3* unless otherwise specified)

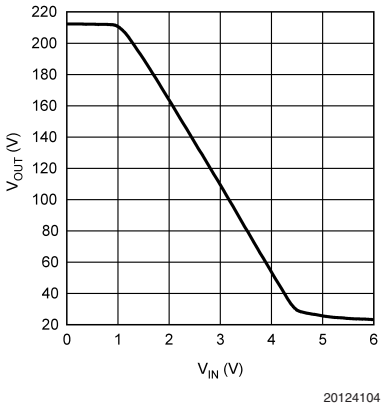


FIGURE 4. V_{OUT} vs V_{IN}

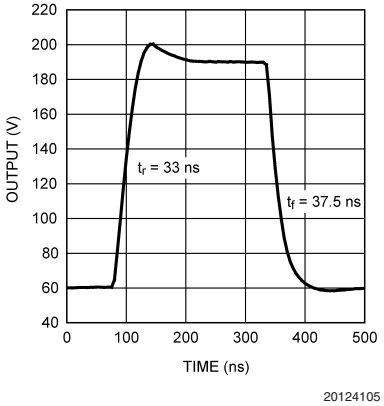


FIGURE 5. LM2425 Pulse Response

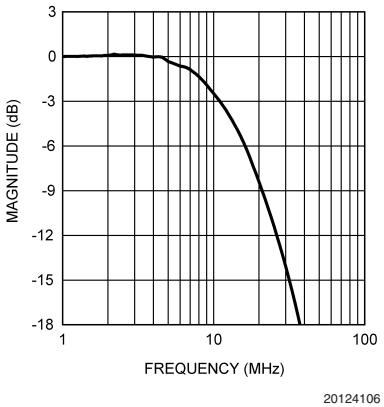


FIGURE 6. Bandwidth

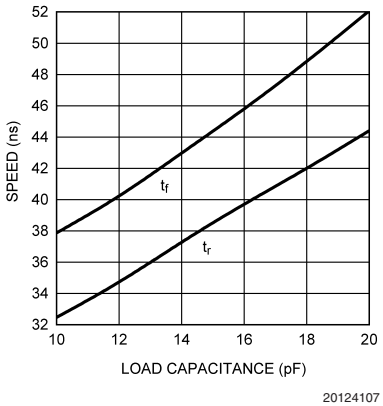


FIGURE 7. Speed vs Load Capacitance

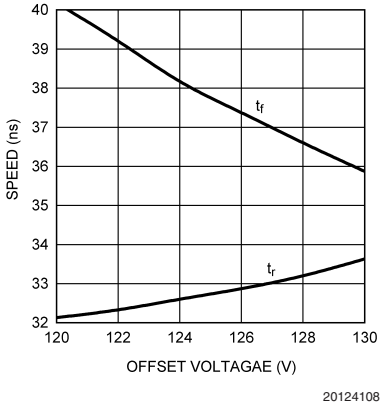


FIGURE 8. Speed vs Offset

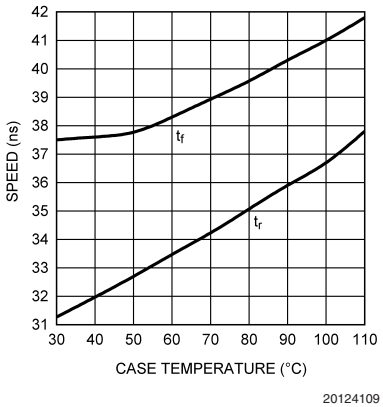


FIGURE 9. Speed vs Case Temperature

Typical Performance Characteristics

(V_{CC} = +220V_{DC}, V_{BB} = +12V_{DC}, C_L = 10 pF, V_{OUT} = 130V_{PP} (60V – 190V), T_C = 60˚C, Test Circuit — *Figure 3* unless otherwise specified)

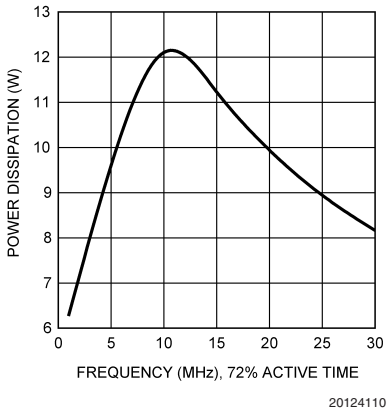


FIGURE 10. Power Dissipation vs Frequency

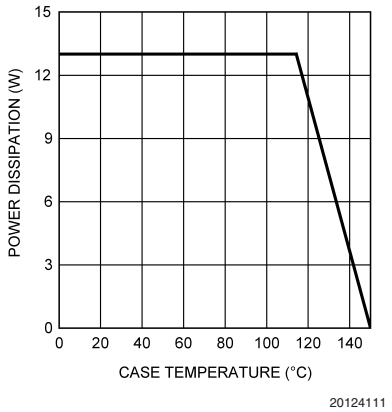


FIGURE 11. Safe Operating Area

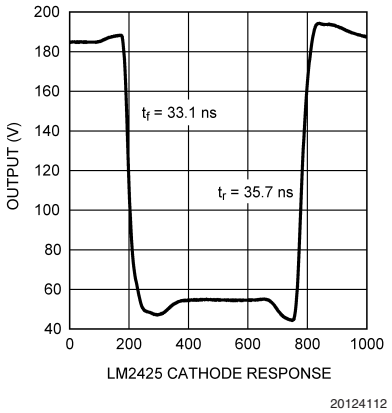


FIGURE 12. LM2425 Cathode Response

Theory of Operation

The LM2425 is a high voltage monolithic three channel CRT driver suitable for DTV applications. The LM2425 operates with 220V and 12V power supplies. The part is housed in the industry standard 11-lead TO-220 molded plastic power package with thin leads for improved metal-to-metal spacing.

The circuit diagram of the LM2425 is shown in *Figure 2*. The PNP emitter follower, Q5, provides input buffering. Q1 and Q2 form a fixed gain cascode amplifier with resistors R1 and R2 setting the gain at –53. Emitter followers Q3 and Q4 isolate the high output impedance of the cascode stage from the capacitance of the CRT cathode, which decreases the sensitivity of the device to load capacitance. Q6 provides biasing to the output emitter follower stage to reduce cross-over distortion at low signal levels.

Figure 3 shows a typical test circuit for evaluation of the LM2425. This circuit is designed to allow testing of the LM2425 in a 50Ω environment without the use of an expensive FET probe. In this test circuit, the two 4.99 kΩ resistors form a 400:1 wideband, low capacitance probe when connected to a 50Ω coaxial cable and a 50Ω load (such as a 50Ω oscilloscope input). The input signal from the generator is ac coupled to the base of Q5.

Application Hints

INTRODUCTION

National Semiconductor (NSC) is committed to provide application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes may be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are also critical to achieving maximum performance.

IMPORTANT INFORMATION

The LM2425 performance is targeted for the DTV market. The application circuits shown in this document to optimize performance and to protect against damage from CRT arc over are designed specifically for the LM2425. If another member of the LM242X family is used, please refer to its datasheet.

POWER SUPPLY BYPASS

Since the LM2425 is a wide bandwidth amplifier, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing or oscillation. 0.1 µF capacitors should be connected from the supply pins, V_{CC} and V_{BB}, to ground, as close to the LM2425 as is practical. Additionally, a 22 µF or larger electrolytic capacitor should be connected from both supply pins to ground reasonably close to the LM2425.

ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. This fast, high voltage, high-energy pulse can damage the LM2425 output stage. The application circuit shown in *Figure 13* is designed to help clamp the voltage at the output of the LM2425 to a safe level. The clamp diodes, D1 and D2, should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. 1SS83 or equivalent diodes are recommended. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor (C3 in *Figure 13*). The ground connection of D2 and the decoupling capacitor should be very close to the LM2425 ground. This will significantly reduce the high frequency voltage transients that the LM2425 would be subjected to during an arc over condition. Resistor R2 limits the arc over current that is seen by the diodes while R1 limits the current into the LM2425 as well as the voltage stress at the outputs of the device. R2 should be a ½W solid carbon type resistor. R1 can be a ¼W metal or carbon film type resistor. Having large value resistors for R1 and R2 would be desirable, but this has the effect of increasing rise and fall times. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2425 would be subjected to. The inductor will not only help protect the device but it will also help minimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 13*.

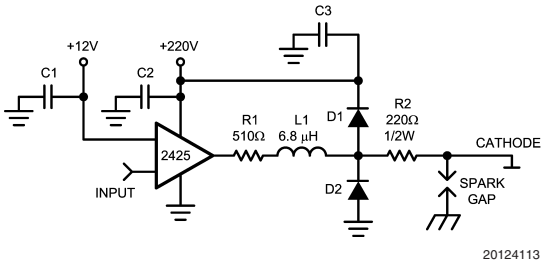


FIGURE 13. One Channel of the LM2425 with the Recommended Application Circuit

EFFECT OF LOAD CAPACITANCE

Figure 7 shows the effect of increased load capacitance on the speed of the device. This demonstrates the importance of knowing the load capacitance in the application. Increasing the load capacitance from 10 pF to 20 pF adds about 12 ns to both the rise and fall times. It is important to keep the board capacitance as low as possible to maximize the speed of the driver.

EFFECT OF OFFSET

Figure 8 shows the variation in rise and fall times when the output offset of the device is varied from 120V to 130V_{DC}. The rise time increases less than 2 ns when the offset is changed from 120V to 130V. The fall time has about a ±3 ns. Variation from the 125V center point, increasing in speed with more offset voltage.

THERMAL CONSIDERATIONS

Figure 9 shows the performance of the LM2425 in the test circuit shown in *Figure 3* as a function of case temperature. The figure shows that the rise time of the LM2425 increases by approximately 19% as the case temperature increases from 30˚C to 110˚C. This corresponds to a speed degradation of 1.9% for every 10˚C rise in case temperature. The fall time has a smaller increase of about 12% over this temperature range.

Application Hints (Continued)

Figure 10 shows the maximum power dissipation of the LM2425 vs. Frequency when all three channels of the device are driving into a 10 pF load with a $130V_{P-P}$ alternating one pixel on, one pixel off. The graph assumes a 72% active time (device operating at the specified frequency), which is typical in a TV application. The other 28% of the time the device is assumed to be sitting at the black level (190V in this case). This graph gives the designer the information needed to determine the heat sink requirement for his application. The designer should note that if the load capacitance is increased the AC component of the total power dissipation would also increase.

The LM2425 case temperature must be maintained below 110˚C. If the maximum expected ambient temperature is 60˚C and the maximum power dissipation is 12W (from *Figure 10*, 10 MHz) then a maximum heat sink thermal resistance can be calculated:

$$R_{TH} \quad \frac{110^oC - 60^oC}{12.1} = 4.1^oC/W$$

This example assumes a capacitive load of 10 pF and no resistive load. The designer should note that if the load capacitance is increased the AC component of the total power dissipation will also increase.

OPTIMIZING TRANSIENT RESPONSE

Referring to *Figure 13*, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz. Ferrite core inductors from J.W. Miller Magnetics (part # 78FR--K) were used for optimizing the performance of the device in the NSC application board. The values shown in *Figure 13* can be used as a good starting point for the evaluation of the LM2425. Using a variable resistor for R1 will simplify finding the value needed for optimum performance in a given application. Once the optimum value is determined the variable resistor can be replaced with a fixed value. Due to arc over considerations it is recommended that the values shown in *Figure 13* not be changed by a large amount.

Figure 12 shows the typical cathode pulse response with an output swing of $130V_{PP}$ inside a modified Sony TV using a Sony pre-amp.

PC BOARD LAYOUT CONSIDERATIONS

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the signal inputs to the LM2425 and from the LM2425 to the CRT cathode should be as short as possible. The following references are recommended:

Ott, Henry W., “Noise Reduction Techniques in Electronic Systems”, John Wiley & Sons, New York, 1976.

“Video Amplifier Design for Computer Monitors”, National Semiconductor Application Note 1013.

Pease, Robert A., “Troubleshooting Analog Circuits”, Butterworth-Heinemann, 1991.

Because of its high small signal bandwidth, the part may oscillate in a TV if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input circuit wiring should be spaced as far as possible from output circuit wiring.

TYPICAL APPLICATION

A typical application of the LM2425 is shown in the schematic for the NSC demonstration board in *Figure 14*. Used in conjunction with an LM1246 preamplifier, a complete video channel from input to CRT cathode can be achieved. Performance is ideal for DTV applications. The NSC demonstration board can be used to evaluate the LM2425 combination with the LM2485 and the LM1246 in a TV.

It is important that the TV designer use component values for the driver output stage close to the values shown in *Figure 14*. These values have been selected to protect the LM2425 from arc over. Diodes D1, D2, D4, and D7–D9 must also be used for proper arc over protection. The NSC demonstration board can be used to evaluate the LM2425 in a TV. If the NSC demonstration board is used for evaluating the LM2425, then U3, the +5V voltage regulator may be used, eliminating the need to route +5V to the neck board for the LM1246.

NSC DEMONSTRATION BOARD

Figure 15 shows the routing and component placement on the NSC LM242X/LM124X/LM2485 demonstration board. This board provides a good example of a layout that can be used as a guide for future layouts. Note the location of the following components:

- C19—V_{CC} bypass capacitor, located very close to pin 2 and ground pins
- C20—V_{BB} bypass capacitor, located close to pin 11 and ground
- C46, C48—V_{CC} bypass capacitors, near LM2425 and V_{CC} clamp diodes. Very important for arc protection.

The routing of the LM2425 outputs to the CRT is very critical to achieving optimum performance. *Figure 16* shows the routing and component placement from pin 10 (V_{OUT1}) of the LM2425 to the blue cathode. Note that the components are placed so that they almost line up from the output pin of the LM2425 to the blue cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components. Note also that D8, D9, R24, and D6 are placed to minimize the size of the video nodes that they are attached to. This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The anode of protection diode D8 is connected directly to a section of the ground plane that has a short and direct path to the LM2425 ground pins. The cathode of D9 is connected to V_{CC} very close to decoupling capacitor C7 which is connected to the same area of the ground trace as D8. The diode placement and routing is very important for minimizing the voltage stress on the LM2425 during an arc over event.

This demonstration board uses large PCB holes to accommodate socket pins, which function to allow for multiple insertions of the LM2425 in a convenient manner. To benefit from the enhanced LM2425 package with thin leads, the device should be secured in small PCB holes to optimize the metal-to-metal spacing between the leads.

Application Hints (Continued)

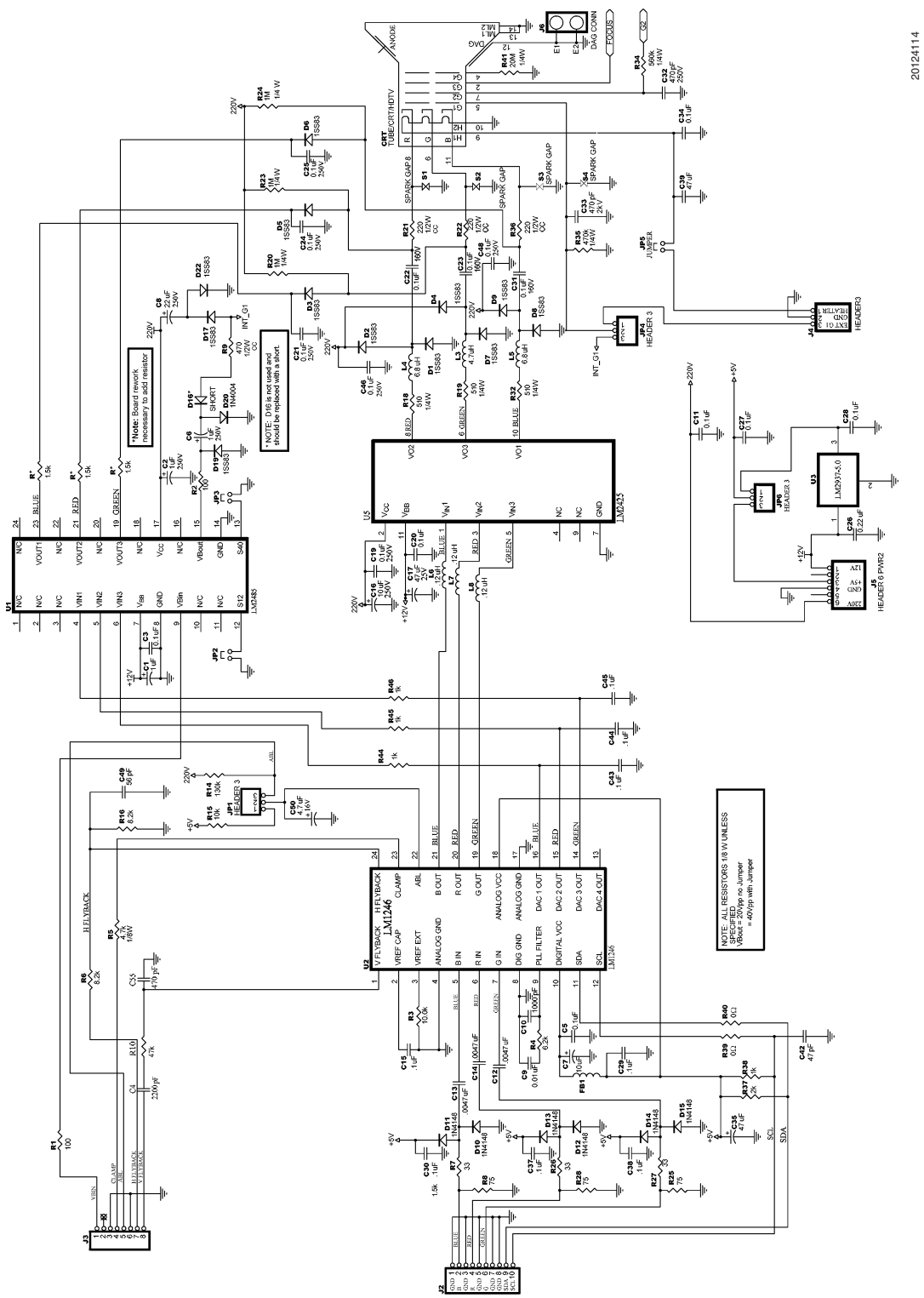


FIGURE 14. LM2425/LM1246/LM2485 DTV Applications Circuit

Application Hints (Continued)

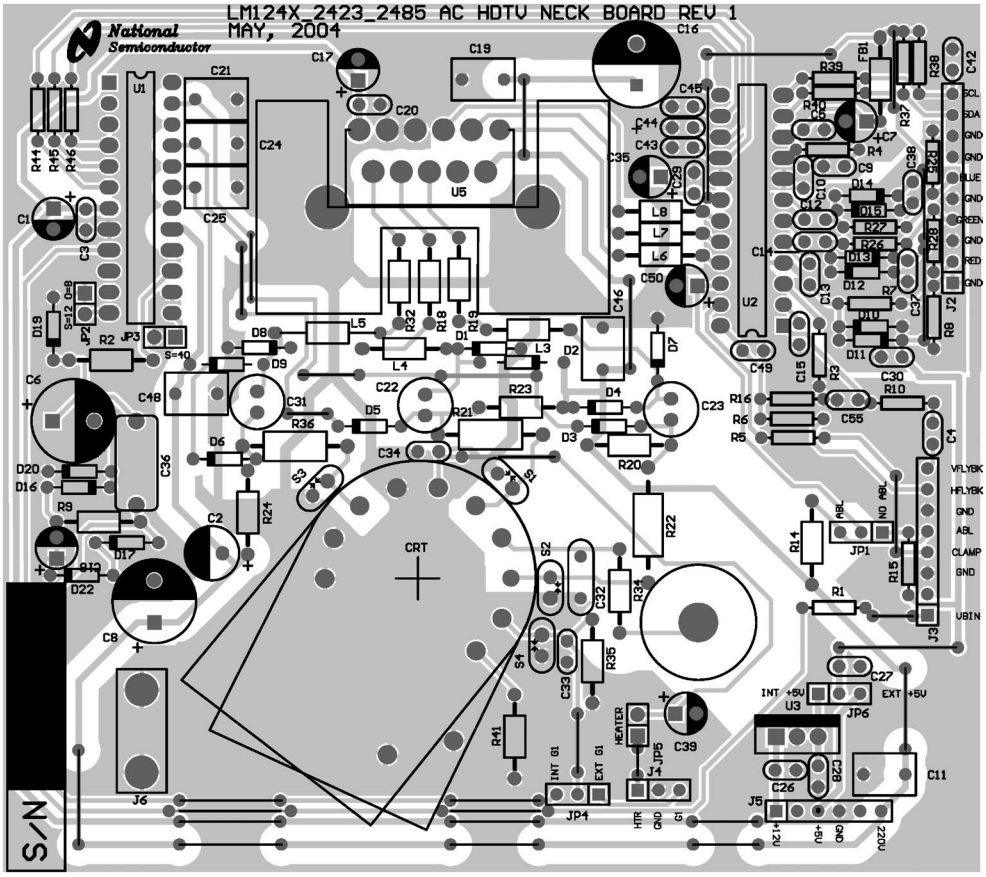


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FIGURE 15. LM242X/LM124X/LM2485 DTV Demonstration Board Layout

Application Hints (Continued)

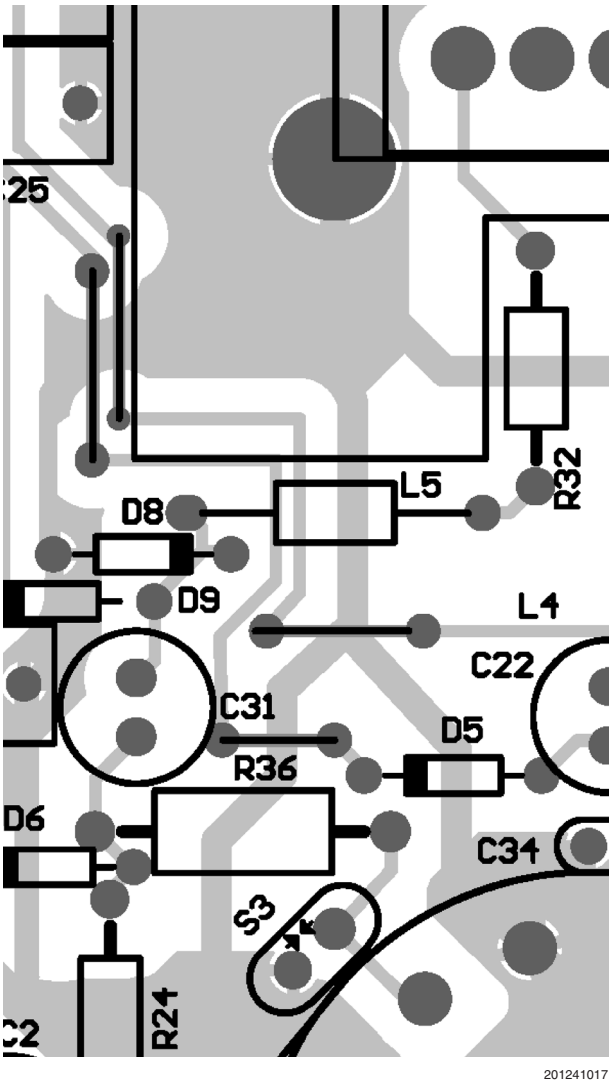
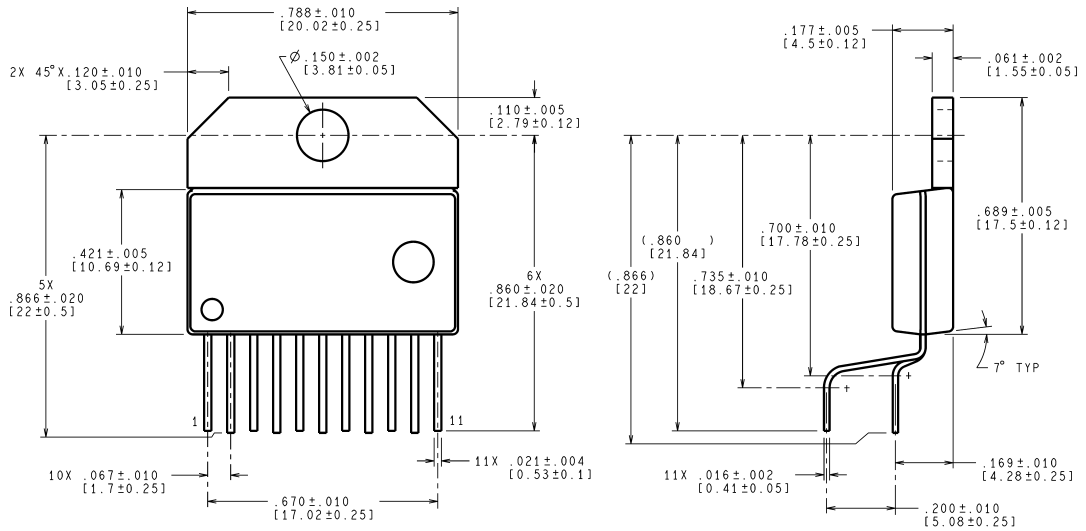


FIGURE 16. Trace Routing and Component Placement for Blue Channel Output

Physical Dimensions inches (millimeters) unless otherwise noted



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NOTE: Available only with lead free plating

NS Package Number TE11B
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